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# MSMP TIMER TESTING AND PROGRAMMING INSTRUMENT

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This report describes a portable instrument designed to program and to test an airborne electronic multifunction timer-controller unit. This instrument programs the erasable and electrically programmable memories--EPROM's, used in the timer, with the necessary flight information. The performance of the timer can also be tested using this instrument.

The report has three major divisions. The first section provides an overview of the instrument. The second part deals with circuit and operational details. The last section gives recommendations and conclusions for future instruments. Sketches of circuits and component layouts are also given.

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# CHAPTER I

## INTRODUCTION

A portable programmer has been designed to store information in the INTEL 2708 erasable and electrically reprogrammable read only memory (EPROM). Four INTEL 2708 units may be manually programmed at one time. The programming is accomplished in two steps. First a volatile random access memory (RAM) is manually programmed, then the information is automatically transcribed into the EPROM's. These EPROM's are used to store a required sequence of events to be reproduced in flight by a rocket-borne timer designed for the MSMP program. Therefore, the programmer has been designed not only to program the memories, but also to test the operation of the timer.

### A. RAM Programming

Each INTEL 2708 EPROM can accept 8192 bits of information organized into 1024 eight-bit words. These words are accessible through ten address lines. Data to be programmed are presented, 8-bits in parallel, to the data input lines. After address and data set-up, a program pulse partially stores the information into the memory. To obtain a complete information transfer, this process of one program pulse per address, must be repeated sequentially at each of the 1024 locations until at least 100 ms of cumulative program pulse time at each address has been achieved. Since this process requires at least 256 passes through all addresses, a buffer random access memory (RAM) is used as a temporary storage for the data to be automatically transcribed into the EPROM. The buffer RAM's (one for each EPROM) are arranged in the 1024 word by eight bit organization as in the INTEL 2708 units.

In the programmer the ten address lines of all memories are connected in parallel. The desired address is selected by manipulating ten binary-weighted switches (Figure 1). Then the programmer is instructed to advance to the selected address by depressing an appropriately named switch. Once the selected location has been reached by the address counter, LED indicators above the selected switches light. Also, four seven-segment LED's display that address as a decimal number.

The data to be stored into the buffer memories are presented to one RAM at a time through eight switches. Selection of the RAM unit to be programmed is made by depressing a selector switch an appropriate number of times (1 to 4). The selection is indicated by another LED display. Information is then presented to the RAM by moving the data switches in the UP position for ZERO's to be programmed. This arrangement has been chosen since the ZERO's in the EPROM represent events in the MSMP timer. Thus an event is associated with the UP position of the switch. Following the data set-up, a load command is given which writes the information into the buffer memory. LED indicators connected to the common output lines of the RAM and the associated EPROM show which of the lines contain the information to be later transcribed into the INTEL 2708 unit. It should be noted that during this manual programming process a signal is applied to the appropriate pins of the INTEL 2708 unit receptacles to keep the EPROM output circuits in the high impedance state. Therefore, EPROM's left in their receptacles will not affect the manual programming process. Once the information has been stored at a particular location of the RAM, programming may be continued by moving to a new

address or remaining at the same address but selecting another RAM, if necessary.

Initially, and after each erasure, all bits of the INTEL 2708 unit are in the ONE state. Data are introduced by selectively programming ZERO's into the desired locations. Since program pulses must be applied to all addresses, ONE's must also be presented to the EPROM by the buffer memory, even though no change in the original bit status is required at a particular location. It is expected that in the MSMP timer application an overwhelming majority of the bits will be in the ONE state. Therefore, to minimize the programming effort, it is desirable to preset the buffer RAM to all ONE's before beginning the manual programming process. As before, one RAM at a time is selected to be programmed. All data switches must be put in the down (ONE) position. The write operation must be changed from an asynchronous dc to a synchronized clocked program mode. The preset process is initiated by depressing and holding the load command switch while at the same time giving the advance command to the programmer. At the end of the transfer cycle, which takes 800 milliseconds, the programmer returns to the same address at which the advance command was given.

A similar process may be used to introduce a continuous string of ZERO's on one or more output lines. Initially the programmer is advanced to the address where the first ZERO is to be introduced. Then the address switches are selected to stop the write process at a location where the last ZERO must be stored or where the individual programming must be resumed. Once again the programmer must be put in the clocked program mode. Depressing and holding the load and the advance command switches will transfer the information presented by the data switches into the RAM between the two selected address locations.

It should be noted that the clocked program pulses are present only when the programmer is advancing. As soon as the advance stops a dc level replaces the program pulse. Therefore, the first and the last locations in this program process are programmed by that dc level. Also, if the programmer is not in the clocked mode, but the load switch is depressed while the unit is advancing to a new address, only the start and the stop positions will receive the write commands.

Provisions have been made to allow a transcription of information from an EPROM into any one of the four RAM's. For that purpose a separate EPROM receptacle has been wired such that the address pins are in parallel with the address lines of all other memories, while he output lines are in parallel with the lines coming from the data itches. Once an EPROM is placed into that receptacle it overrides the signals originating at the data switches. Using the procedures described earlier in conjunction with the preset process of a RAM, information from an EPROM, placed into that receptacle, may be transferred into a RAM for editing or further programming.

To prevent an accidental programming of a RAM while checking a program or performing some other work, the write signal paths to the RAM's may be blocked. This is done by moving the select circuit into a position where the select display shows a zero.

The programmed RAM's may be checked by selecting an address, advancing the address counter and observing the LED indicators on the output lines. In an alternate method, the programmer is placed in a read mode where the select circuits are automatically reset into the safe position. In this mode, upon receiving a command to advance, the programmer will proceed until one or more ZERO's are encountered at the outputs of the RAM's. At that time the programmer will stop, display

the address in the binary and the decimal codes and will light the LED indicators on the lines where the ZERO's are present. Once again, an advance command will force the programmer to proceed to the next location where ZERO's are present.

This check can also be run with the stops removed. For that purpose the clock signal which advances the address may be slowed to one Hz when the programmer is switched into the free run condition. The address and the output line LED displays will continue to operate.

B. EPROM Programming

To transcribe the information from the RAM into the EPROM the new programmer is switched into an automatic mode of operation. The selector circuits, used to determine which RAM was to be programmed in the manual mode, are disabled by moving the selector into a program position. In that position the seven-segment selector LED indicator displays a letter P. Also, the write circuits must be switched into the clocked program mode. Advance command initiates the transcription process which continues for 204.8 seconds. When the 256 program loops through, all of the 1024 word locations have been completed, the programmer stops, and a clock, if enabled, displays the elapsed time. The elapsed time display may be used to confirm that the necessary number of loops have indeed been completed.

Once the transcription process has been started most of the control and command circuits become disabled. This was introduced to minimize the possibility of accidental interruptions or data alterations during the relatively long transcription process. The programming may be interrupted without any adverse effects by switching into manual mode, or

transferring out of the clocked program, or by switching into the low frequency clock operation. Switching off the EPROM power will destroy the contents of the loop counter but will not affect the partially stored information. Of course, switching off the main power will erase the information stored in the RAM. In the first two non-destructive interruptions of the programming process the programmer stops and displays the address at which the interruption occurred. The contents of the loop counter also remain intact. Only a reset command, after switching into manual mode, will destroy the contents of this counter. Therefore, returning the programmer to the proper mode and instructing it to advance will resume the transfer of information until the required number of loops have been completed. The clock display also will indicate the correct elapsed programming time of 204.8 seconds.

A slightly more serious interruption may be caused by switching the clock into a "slow" operation. In this case the programming process will stop, but the elapsed time clock will continue to run. Therefore, the check on the number of completed loops will be lost and the trust will have to be placed in the performance of the loop counter. Programming will resume as soon as the clock is switched back into the normal mode.

Besides disabling the manual reset and write circuits when the programmer is switched into the automatic mode, other accidental and false program run possibilities also have been minimized. As it was pointed out earlier, it requires a proper setting of the select switch as well as of the clocked program switch to produce data transfer. The letter P in the select display signifies that the loop counter and the program pulse generator circuits have been enabled and that the stop features used in testing have been removed. Also, the advance command cannot be given unless the clocked program switch is in its proper position. This

was done to prevent a program run in which program pulses would be absent. Also, once the programmer starts advancing, the select circuit becomes disabled excluding any possibility of accidental switching of that circuit out of the program mode. It should be noted, that if the programming process is interrupted by a transfer into the manual mode, the select circuits are reset into the safe test position which disables the manual write operation.

To check the programmed EPROM's, the select circuit must be moved from the program position. Once that has been done, the same procedures as described in conjunction with RAM testing may be followed. As long as the programmer remains in the automatic mode the RAM output circuits are kept in the high impedance state. Therefore, the output line LED indicators will be controlled by the state of the EPROM outputs.

Since the programmer will be operated in the field where short duration power losses may occur, a 28 volt 1.2 AHR NiCd battery is included in the unit. This battery is charged whenever external power source is connected to the programmer and it supplies power when the external source fails. This arrangement protects the volatile RAM from losing data and allows for a continuous operation of the programmer over limited time. When prolonged power outages are expected or for overnight preservation of data the information stored in the RAM should be transcribed into an EPROM.

C. Timer Test

The MSMP timer test may be conducted in either of the two manual/automatic modes of operation described in the previous sections. In the program-write mode, stops will occur at the addresses selected by the address switches, while in the read mode, the timer will be stopped

whenever one or more relay drivers are activated. Also, the stops may be removed if the programmer is switched to the free-run operation in the read mode.

Since no provisions have been made to supply a signal which would put the EPROM outputs into the high impedance state during these tests, all EPROM's must be removed from the programmer sockets. Otherwise, permanent damage may be caused to these units when the select display indicates zero, i.e. when the programmer is in the check state.

To connect the MSMP timer for the tests, a shorting plug must removed from the programmer. Removal of this plug puts the output circuits of the RAM's into the high impedance state and disconnects the internal clock from address advance circuits. The clock signal is obtained from the timer thus synchronizing the address counters in the timer and the programmer.

To measure the time interval between events or the total elapsed time during the tests, a clock with a five digit display featuring 0.1 second resolution has been included into the programmer. Every time the programmer inhibits the clock signal in the MSMP timer the programmer clock is also stopped. The clock may be reset independently of other programmer circuits and will start whenever a command is given to the timer to resume operation. Since it may be distracting to have the clock display changing during some operations a provision is included to disable the clock display.

The programmer has circuits to detect a malfunction in any one of the triple redundant sections of the timer. Five functions are monitored by four monitor and display circuits. The monitored signals include three combined signals, each consisting of the most significant bit from one of the timer counters and one of the strobe pulses. During

the first half of the timing period the strobe pulses predominate, while during the second half the counter signals take over. Two other groups of three signals each are the EPROM power switching pulses and the chip deselect pulses. Whenever one of the three signals in each of the above mentioned groups fails to appear in unison with the other two, an LED indicator goes off or starts flashing. There is some diagnostic value in the two modes of error detection, but it would require a lengthy description of the MSMP timer operation before the significance could be explained. The fourth monitor receives pulses from the timer crystal oscillators. A failure to light an LED indicates that one of the two timer oscillator circuits has failed.

Jacks are provided to measure the power supply voltages in the timer. Also included are the timer arm-disarm, start-stop command and monitor circuits.

## CHAPTER II

## CIRCUITS

### A. Clock

The clock of the programmer shown in Figure 2 consists of a crystal oscillator, frequency dividers, gates, control switches, decade counters and seven-segment displays.

The oscillator (QT4C) operates at 20.480 KHz. This frequency is scaled by the binary ripple counter (SCL 4040) to 1280 and 10 Hz. The 1280 Hz signal is used to drive the address generator-counter and the program pulse generator during the clocked program mode. The 10 Hz signal drives the five decade clock counter. The decade counters (SCL 4426) with their 7 segment decoded outputs and the LED displays (FND-70) form the digital clock having a resolution of 0.1 seconds. The primary function of the clock is to display elapsed time during the MSMP timer tests. Therefore, every time the programmer is stopped at a particular address the signal flows through an AND gate to the frequency divider and consequently the clock is inhibited. Count resumes when the programmer advances. The clock may be reset independently from the programmer when an elapsed time measurement between two events is necessary. Of course, the cumulative count is then lost. Also, as it was pointed out earlier in this report, the clock may be used to confirm the loop count during the EPROM programming. Since one loop takes 0.8 seconds to complete, the clock will display 024.8 seconds for the full count of 256 loops. To eliminate a distraction that can be created by the display during manual programming or EPROM testing operations, the display may be turned off. To disable the display the switch S1 is moved to ground

the inputs of the AND gates which transmit signals to the display terminals of the decade counters.

All seven-segment LED displays in the programmer are pulsed at a duty cycle of 0.2. A divide-by-8 counter with decoded outputs (SCL 4022), connected to reset after a count of five, generates the required pulses on five output lines (MUX) which distribute the signals to the various displays. A signal to the monitor circuits is also obtained from that counter.

Switch S2 selects a frequency at which the address generator-counter is advanced. For automatic programming only the 1280 Hz signal can be used. The one Hz signal is blocked in the AND gate during this operation. In some testing operations the one Hz signal may be preferable.

In order to synchronize the address counter with the clock, the one Hz signal is inverted by the NAND gate. The address counter of the programmer advances on the negative going edge of a pulse, while the SCL 4426 unit is triggered on the positive going edge. Therefore, without inversion, a 0.5 second discrepancy would appear between the clock read-out and the address display each time the programmer is advanced from a reset state.

Clock signals to the control section of the programmer are routed through a 50-pin connector which provides the interface between the programmer and the MSMP timer during tests. Therefore, a shorting plug must be provided when programming or testing the memories. Clock signals to the control circuits are obtained from the timer during the timer tests.

## B. Address and Data Circuits

The address and the data generating and monitor circuit diagram may be seen in Figure 3. A counter, data latches, comparators, LED indi-

cators, drivers, and switches are used to select, present and to display the information to be stored in the RAM and/or EPROM.

The address is generated by the binary counter (SCL 4040). The 1280 Hz driving signal for that counter originates in the clock section of the programmer. When necessary, the one Hz signal may also be selected to drive the address generator-counter. When the output of the counter matches the binary word represented by the address switches, the digital comparators (MC 14585) produce a high voltage level at W. This voltage commands the control section of the programmer to interrupt the clock signal to the address counter. Thus the address at which the information will be stored is selected. Each address line having a high voltage level lights an LED indicator. A light for each address switch in the UP position signifies that the desired address has indeed been generated. The address is applied to all EPROM's and RAM's in parallel. Also, the spare socket CC (not shown in the figure) and the socket DD, used to transfer data from EPROM into a RAM, are connected to the address lines.

Data to be written into the RAM is selected by the data switches. Eight data bits are presented in parallel to all four 8k RAM's. The RAM to be loaded receives the write pulse at the R/W terminal from the control section of the programmer. The data lines are also connected to the receptacle reserved for the data transfer from an EPROM into a RAM. The 30k ohm resistors isolate the data lines from the switches and allow the EPROM to override signals originating at these switches.

The outputs of a RAM are connected to the outputs of an EPROM for which the RAM acts as a temporary data storage. The output lines which contain ZERO's force the buffer/drivers (SCL 4441) to light LED indicators. This provides a check on the data stored in the RAM during the manual programming cycle. In the automatic mode the indicators

display the EPROM output line status. The control signals, ONE for high impedance state and ZERO for the READ state, are generated in the control section of the programmer and are applied to the $\overline{CS}$ and $\overline{CE}$ terminals at appropriate times.

The output lines are also connected to the 50-pin interface connector and the ZERO detection circuit formed by the AND gates. Whenever a low level signal appears on one or more of the output lines a ONE is generated at the output of that circuit. This signal is used to inhibit the clock when the programmer is operated in the READ mode during the EPROM or the timer tests. Resistors connect the output lines to the five-volt supply. These resistors serve as loads for the relay driver circuits of the MSMP timer during tests. Also, they serve as pull-up resistors for the LED drivers when the EPROM's are removed from receptacles while the programmer is in the automatic mode.

## C. Control Circuits

Control over the various modes of operation of the programmer is exercised through the circuits shown in Figure 4. The control circuits were designed to provide reasonable protection against an accidental erasure or an introduction of unwanted data into the memories. Circuits, not needed for a particular phase of programming or testing and posing a potential hazard, if activated, are disabled during these operations. Also, all automatic processes which affect a series of memory locations must be initiated by more than one command.

Control of the programmer centers around a D-type flip flop (Za). In its RESET state the unit inhibits clock signals in the clock section of the programmer, as well as at the AND gate (Z3-11)*. During the

*ZN-M should be read: gate N, pin M.

MSMP timer tests an inhibit signal is also sent to the timer circuits.

Depressing the ADVANCE switch sets the flip flop. The clock signal passes through the AND gate and triggers a monostable. This circuit produces signals to advance the address and the address display counters (SCL 4040 and SCL 4426 respectively). The address counter is triggered on the negative going edge while the display counter responds to the leading edge of a clock signal. The two out of phase signals produced by the monostable advance the two counters at the same time. While the SCL 4040 generates binary address words, the four SCL 4426 decade counters driving the FND-70 seven segment LED's display the address as a decimal number. Thus, a simple binary to decimal conversion is achieved.

The inverter in the monostable clock circuit synchronizes the clock display in the programmer, the MSMP timer clock and the programmer address counter. Without the inverter, the leading edge triggered monostable circuit would introduce a one-half clock period discrepancy between the address counters in the programmer and the timer. The monostable was introduced to provide some delay between the program pulse, which is derived from the main clock, and the advance of the address counter during programming operations. The address and the display counters are reset on the 1024th count through Z6-4 by a pulse originating in the address counter.

The signal flow to the address counters is interrupted by resetting Za. This may be done by depressing the RESET switch. That command, of course, resets the whole programmer. It should be noted, that the RESET switch is disabled when the programmer is in the AUTO mode. During programming and testing operations Za is reset through the clock terminal (pin 3) on the positive going edge of a pulse. This pulse

may originate either at the digital address comparator circuit (W) or at the circuit which detects the presence of ZERO's on the output lines of the memories (R). When it is desired to stop the programmer at a selected address the READ/WRITE switch must be in the WRITE (W) position. Then the stop pulse arrives at Za from the digital comparator. Since the SCL 4040 operates as a ripple counter, short duration pulses are generated at the comparator during the major transitions in the counter. The 1000 pF capacitor eliminates these false stop signals.

When ZERO's are to be detected the READ/WRITE switch should be in the READ position. ZERO's on the output lines produce a ONE at Z3-9. A string of consecutive ZERO's keep the input to that gate high. Since Za responds only to the positive going clock transitions, this dc signal would remain undetected. The monostable (Zc) produces a negative going pulse every time the address counter advances. This forces the output of the AND gate to produce transitions when a high level signal is produced by the ZERO detector at the other input of the gate. The stop signal may be ignored by putting the RUN/STOP switch in the RUN position. This mode of operation may be useful during the EPROM or MSMP timer tests.

During manual operation the RAM to be programmed is selected by depressing the SELECT switch. The resulting signal advances the SCL 4022 (Zd) and SCL 4426 (Ze) counters by one count each time the switch is depressed. The Zd unit is an octal counter/divider with decoded outputs, while the Ze circuit is the already familiar decade counter/LED display driver. The output of the octal counter enables one of the four NAND gates (Z1). Depressing the LOAD switch produces a ZERO at the output of the selected gate. This represents a write command which transfers the information stored in the data switches into the selected RAM. The selection (1 to 4) is displayed by the FND-70 driven by Ze.

Both the LOAD and the SELECT switches receive their dc voltage from Za. Pin 2 of Za produces a low voltage when the address counter is advancing. Therefore, the selection switch and partially the loading switch are disabled during that time. If the LOAD switch were depressed, only two RAM locations would be programmed: the starting and the end of the run addresses.

When it is necessary to preset a RAM to all ONE's or ZERO's, selection is made in the manner just described. The programming then may be done automatically by putting the PROGRAM switch in the appropriately named position, depressing and holding the LOAD switch and, at the same time, activating the ADVANCE switch. Clock pulses from Z3-11 will propogate through Z5-4 and Z3-4, provided the AUTO/MAN switch is in the MAN position. In this mode all locations including the starting and the end addresses will be loaded with the information present in the data select switches. To complete one cycle of preset programming takes only 0.8 seconds. This step to preset the four RAM's to all ONE's should be taken every time a program for the MSMP timer must be written. This is the logical conclusion considering that only ZERO's need be programmed into the EPROM's and that the non-events (ONE's) on the 32 output lines of the timer by far excede the number of events. If, by chance, the opposite were true, the RAM's could be preset to all ZERO's before the start of the programming process.

When the select indicator displays a zero, the write circuits to the RAM's are disabled since all inputs to the NAND gates (Z1) receive a low signal from the SCL 4022 unit. This state is recommended when checking the program or the MSMP timer in the WRITE mode, and when the contents of the RAM must be protected for a possible later use. In the READ mode the select counter is automatically reset to the zero

state through the OR gates Z6-8 and Z6-11. This counter also resets to zero after the fifth select command when operating in the manual mode.

To transcribe information into the EPROM's the programmer is switched into the AUTO mode. The select circuit is advanced until a letter P appears in the select display. The PROGRAM switch is moved into the programming position and the ADVANCE switch is depressed.

The select counter SCL 4022 produces a logical ONE at pin 4. This voltage enables a number of gates. The AND gate Z2-4 in conjunction with the 2N2222 transistor drives the FND-70 to display the letter P. Gate Z3-3 transmits the clock signals to the program pulse generator while the gate Z5-10 applies a continuous high voltage level to Za-3 thereby effectively inhibiting stop signals originating at the digital comparator. Gate Z2-11 transmits pulses to the program loop counter Zf-10. These pulses originate at the address counter: one pulse every time the counter is reset. After 256 loops the counter Zf-12 generates a pulse which through the gates Z5-3 and Z6-9 resets Za-4 and Zd-15, thus terminating the programming cycle. Since the loop counter does not reset itself, LOAD, SELECT and ADVANCE commands remain inhibited. To resume normal operation the programmer must be transferred into the manual mode and then reset.

Both the letter P in the select display and the PROGRAM switch must be properly set to transcribe information into the EPROM's. When the PROGRAM switch is off but the select counter has been properly set, the programmer will not advance. High voltage level form Zd-4 through the gates Z5-11 and Z5-3 resets the Za-4. This signal is also transmitted through the 100k resistor and the 1N4148 diode to the ADVANCE switch where it charges the 1000 pF capacitor. Therefore the switch

commands to advance are ignored by the circuit. When the PROGRAM switch is closed it shunts the signal from Zd-4 to ground allowing the circuit to resume normal operation.

When the PROGRAM switch is closed but the P state has not been selected and a command is given to advance, the programmer cycles once to the starting address and stops. Of course, no program pulses will be present and the loop counter will remain reset. It should be noted that before attempting to program, a reset signal should be applied to the programmer before switching into AUTO mode. This assures that the loop counter is reset to zero and prevents a possible short programming run.

To test EPROM's the programmer must be kept in the AUTO mode; otherwise the procedures and circuit operation are similar to the ones used in RAM tests. Since the RAM's and the EPROM's share common output lines, signals are generated at their respective chip select terminals ($\overline{CS}$ and $\overline{CE}$) to produce appropriate output states during the various modes of operation. When in manual mode a +5V level is generated by the two-transistor circuit at the EPROM ($\overline{CS}$) terminal. This produces a high impedance state. At the same time a zero volt signal appears at the ($\overline{CE}$) terminal of the RAM allowing it to control the output lines. During EPROM programming in the AUTO mode +12 volts are generated at $\overline{CS}$ while the $\overline{CE}$ remains at zero. When the select counter is in other than the program position, +5 volts are applied to the RAM and zero volts to the EPROM chip select terminal. In this case the EPROM controls the output lines. The zener circuit receives its power from the RAM supply and applies +5 volts to the EPROM $\overline{CS}$ pins when the programmer power is shut-off during removal or insertion of the memories while the RAM's are inactive.

During the MSMP timer tests the shorting 50-pin connector is

replaced by a test connector. This breaks the programmer clock path and connects the timer clock to the address counter. Also, the RAM is placed into a high impedance state. EPROM's MUST BE REMOVED from the receptacles during the timer tests to prevent shorting of their outputs to ground. Otherwise, the programmer circuits operate the same way as during the EPROM or the RAM tests.

D. Program Pulse Generator

To program the INTEL 2708 EPROM the Chip Select ($\overline{CS}$/WE) pin must first be raised to +12 volts and then a program pulse must be applied to the program input. The program pulse amplitude must be maintained between 25 and 27 volts, it must be less than one millisecond in duration and it must have the rise and the fall times between 0.5 and 2 microseconds. To generate the required pulse the circuit show in Figure 5 has been constructed.

A clock pulse at A saturates the 2N2709 transistor and allows the 100 pF capacitor to charge through the 5.6k resistor with a rise time of 1.2 μs. The zener-diode circuit clamps the capacitor voltage at 27.2 volts while the output transistors 2N2222 drop the pulse voltage to approximately 26 volts. During that time the diode (1N4148) and the transistor (2N2907) circuit do not conduct. At the end of the clock pulse this circuit discharges the capacitor maintaining 1.2 μs fall time.

The output circuit contains an eight milliampere current source. This circuit is necessary to absorb the current sourced by the EPROM's (up to 2 ma per unit) whenever the Chip Select terminal is raised to +12 volts. In the absence of the program pulse, this circuit maintains the output voltage slightly below zero volts. If only a resistor were used, the voltage developed by the EPROM current would subtract from the program

pulse amplitude creating a situation where underprogramming could result.

The program pulse generator maintains the program pulse specifications when programming from one to four EPROM's.

E. Monitor Circuits

A number of monitor circuits indicate the status of the programmer and/or the MSMP timer. The circuits are shown in Figure 6.

LED indicators are used to show when the programmer is in the AUTO, the WRITE and the PROGRAM modes. The AUTO (AT) indicator is self-explanatory. The write (WR) indicator lights whenever the programmer is in a state where data transfer may take place: the READ/WRITE switch is in WRITE position and the select circuit is not in the safe (zero) state. The program (PG) LED flashes whenever the PROGRAM switch is in the programming position. The flashing signal is obtained from a counter (CLK) driven by the MUX signal. This same signal is used to flash the timer redundancy and clock monitor circuits.

Nine signals from the MSMP timer are used to provide indication that all three redundant circuits in the timer are functioning in unison. EPROM power pulses and chip select pulses are monitored separately by two out of the three identical redundancy monitor circuits. The circuits consist of a D-type flip flop driven by a clock signal and a signal originating at the EXCLUSIVE OR circuit. When one of the three input pulses fails to appear in unison with the other two, a reset is generated at the D-type flip flop which causes the LED indicator to go off. The clock signal again sets the flip flop and lights the LED. Thus the flashing failure indication is obtained. A high level signal at the reset terminal overrides the clock signal and extinguishes the LED permanently. Capacitors at the outputs of the EXCLUSIVE OR gates remove short duration

pulses caused by differing propogation delays in the timer circuits.

The third circuit monitors three combined signals, each consisting of the MSB of the timer counters and the data latch strobe pulses. These two signals are combined in the timer through OR gates. During the first half of the timer test the MSB's of the counters are low. Therefore, the strobe pulses are transmitted. During the second half of the test the counter signals predominate.

To monitor the dual redundant timer clock, pulses from the MSMP timer continuously reset a D-type flip flop causing a LED indicator (CL) to light. The monitor clock sets the flip flop and extinguishes the LED. Since the MSMP timer clock rate is much higher than the monitor clock, the short periods during which the LED is forced off by the monitor clock are undetected by the eye.

To complete the MSMP timer redundancy monitor system, jacks are provided in the programmer to measure the supply voltages. The dual supplies of -5, +5, and +12 volts are combined through resistors and brought out to the three programmer jacks. Voltages different from the nominal values indicate problems in the timer supply.

Switches and LED indicators are also provided to test the timer arming and starting relays. When testing, these switches should be used to reset the timer. To start the timer the ADVANCE switch in the programmer must be depressed. This removes the clock inhibit signal from the timer and synchronizes the timer with the programmer elapsed time clock.

### F. Power Circuits

Separate DC-DC converters are used to supply power to the RAM and to the EPROM-programmer circuits (Figure 7). To prevent damage to the EPROM's while inserting and removing them from the receptacles a switch

is provided to disconnect power from the programmer circuits, while the volatile RAM continues to receive power.

A battery has been included to supply power to the programmer during power outages. Use of an available 28.8 volt 1.2 Ahr standby battery requires a voltage regulator and switchover circuits. Otherwise the battery could not be maintained at a full charge while externally supplying the DC-DC converters with the required 24 to 32 volts. The voltage regulator circuit allows the external supply to be operated at 34 to 36 volt levels when charging of the standby battery is desired. To charge the battery at the recommended 120 mA the external supply should be set at 35 volts. A 40 mA trickle charging current may be maintained indefinitely.

The switchover circuit consisting of the TIP36 and the 2N2907 transistors provides for a smooth transition to the battery operation when the external supply falls below 26 volts. The battery provides up to one hour of full operation. Switching the EPROM supply off prolongs the operating time, but in the case of power failure, it is recommended that the contents of the RAM be transcribed into the EPROM's for preservation. To reload the RAM from the EPROM's takes very little time.

# CHAPTER III

## CONCLUSION

The portable programmer-tester has been designed to provide the field support personnel with a light-weight, easy-to-operate instrument. Safeguards against accidental erasures or introduction of erroneous data into the memories have been provided within practical limits.

External dc power source and an internal dc-dc conversion to supply the variety of voltages to the circuits was chosen over a built-in ac to dc conversion system. An ac to dc conversion system would add weight and size to the electronics system and would provide less ac isolation. Since dc sources at the voltage and current levels required by the instrument are commonly available during field operations, the shipping weight is reduced.

Programming process of the RAM is relatively simple. Once preset, only the even addresses need be programmed. Visual check of the data stored in the memory is available the instant the data is entered. Therefore, errors may be quickly corrected. The binary address selection, in conjunction with the monitor LED's, provides the operator with a direct comparison between the address line status and the switch selection. The decimal address display provides an additional check.

The transcription process of data from RAM into EPROM is quite well protected against accidental destruction. Practically, only switching off the key-operated main power switch may destroy the data in the RAM. A built-in battery protects against power failures.

When testing EPROM's or checking the RAM's the data is accessible within 0.8 seconds to be displayed by monitor LED's. Also, during MSMP

timer tests the timing process may be stopped at any desired address. Monitors to detect failure in one of the triple redundant circuits in the counter section or in the dual redundant power circuits of the timer have been provided.

It could be recommended that future designs incorporate a decimal switch addressing system. It would require a decimal-to-binary-to-decimal display conversion to achieve the same level of reassurance provided by the present instrument. Although more complex than the present system, it would remove from the person writing a program the burden of conversion from the decimal address number to the switch code. Also, only four switches would have to be manipulated by the operator to address the memories. In addition, the UV EPROM eraser and battery monitor circuits could be included in the new instruments.

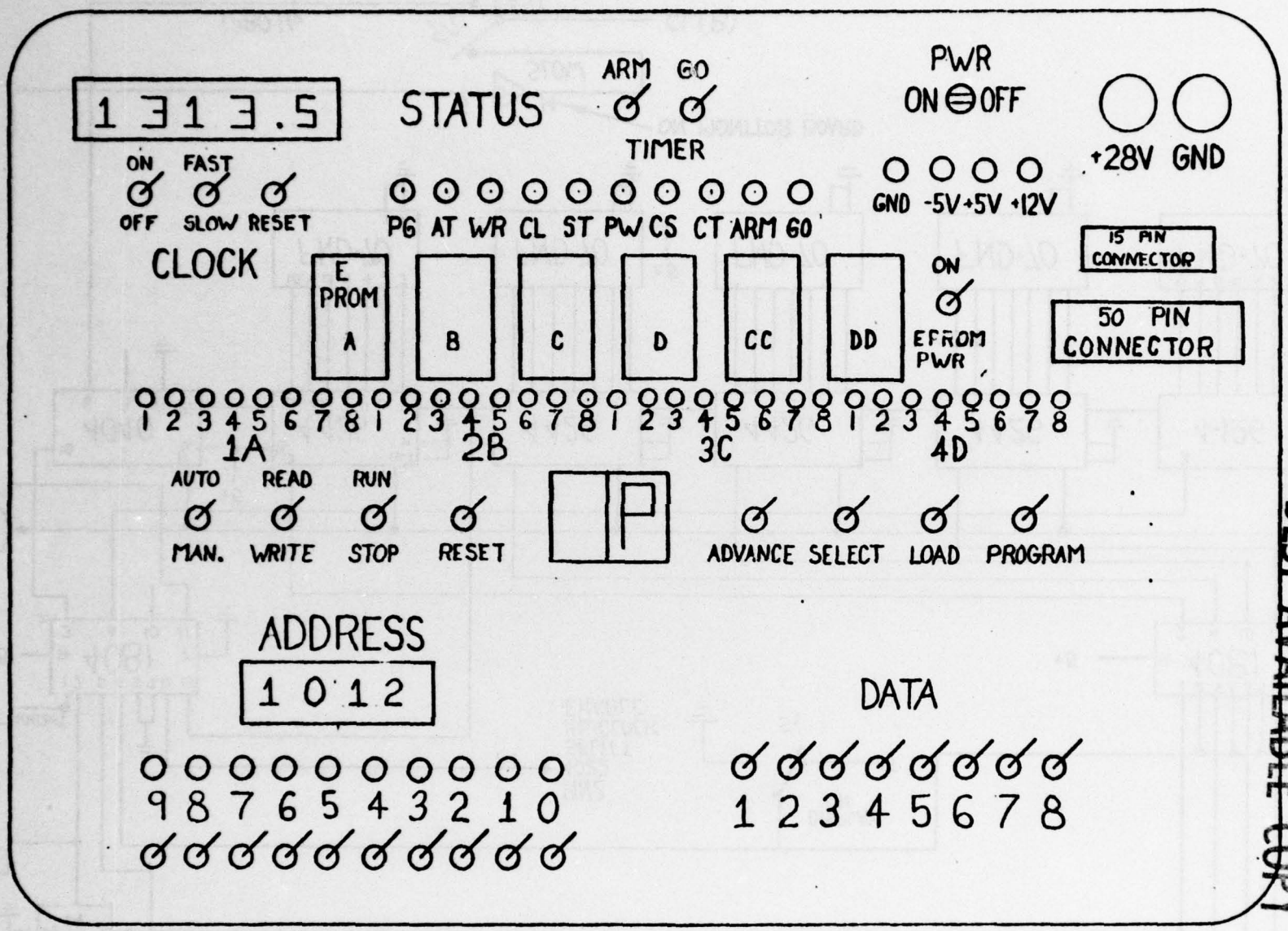


FIGURE No. 1. PROGRAMER

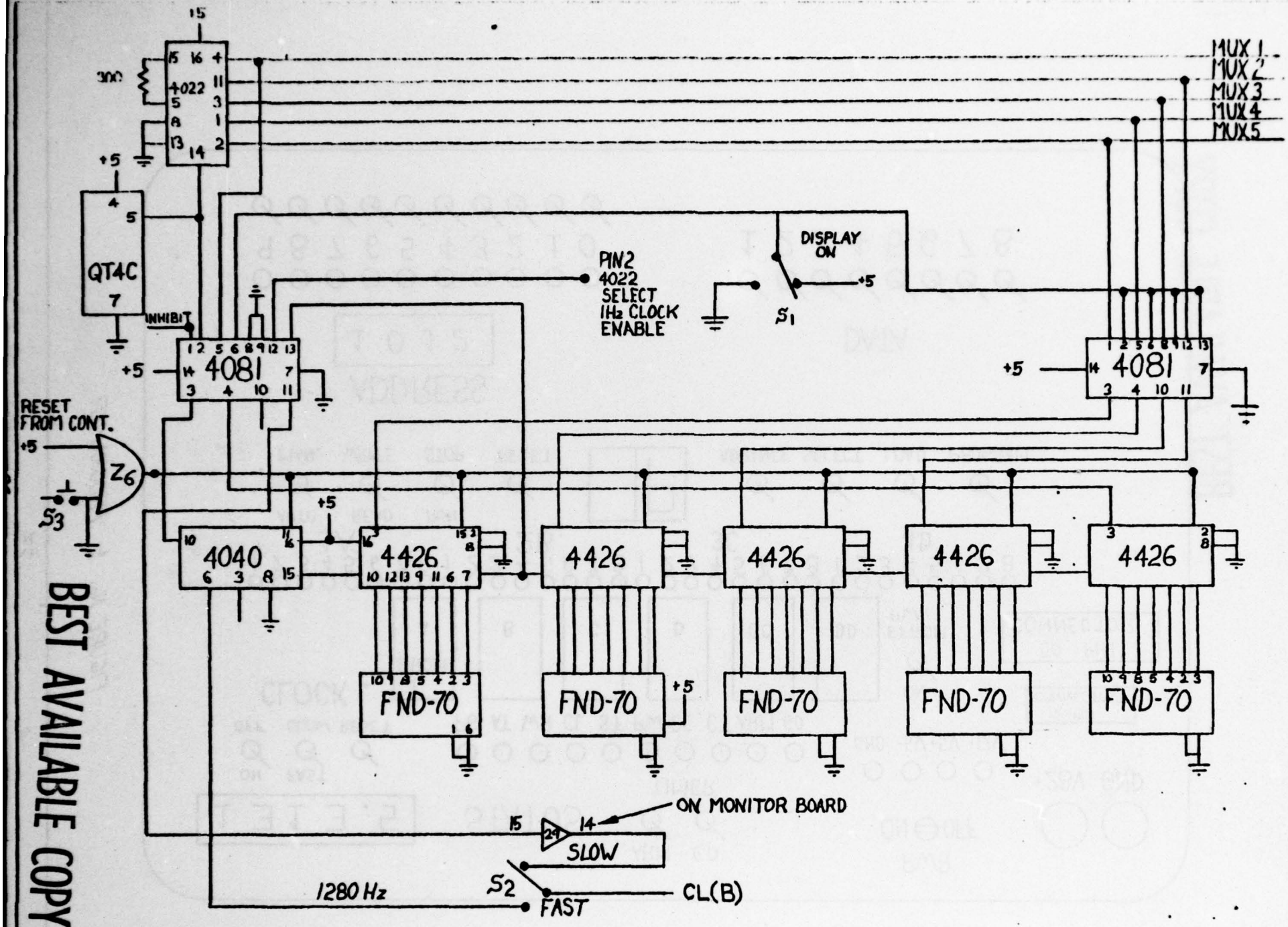


FIGURE No. 2. CLOCK

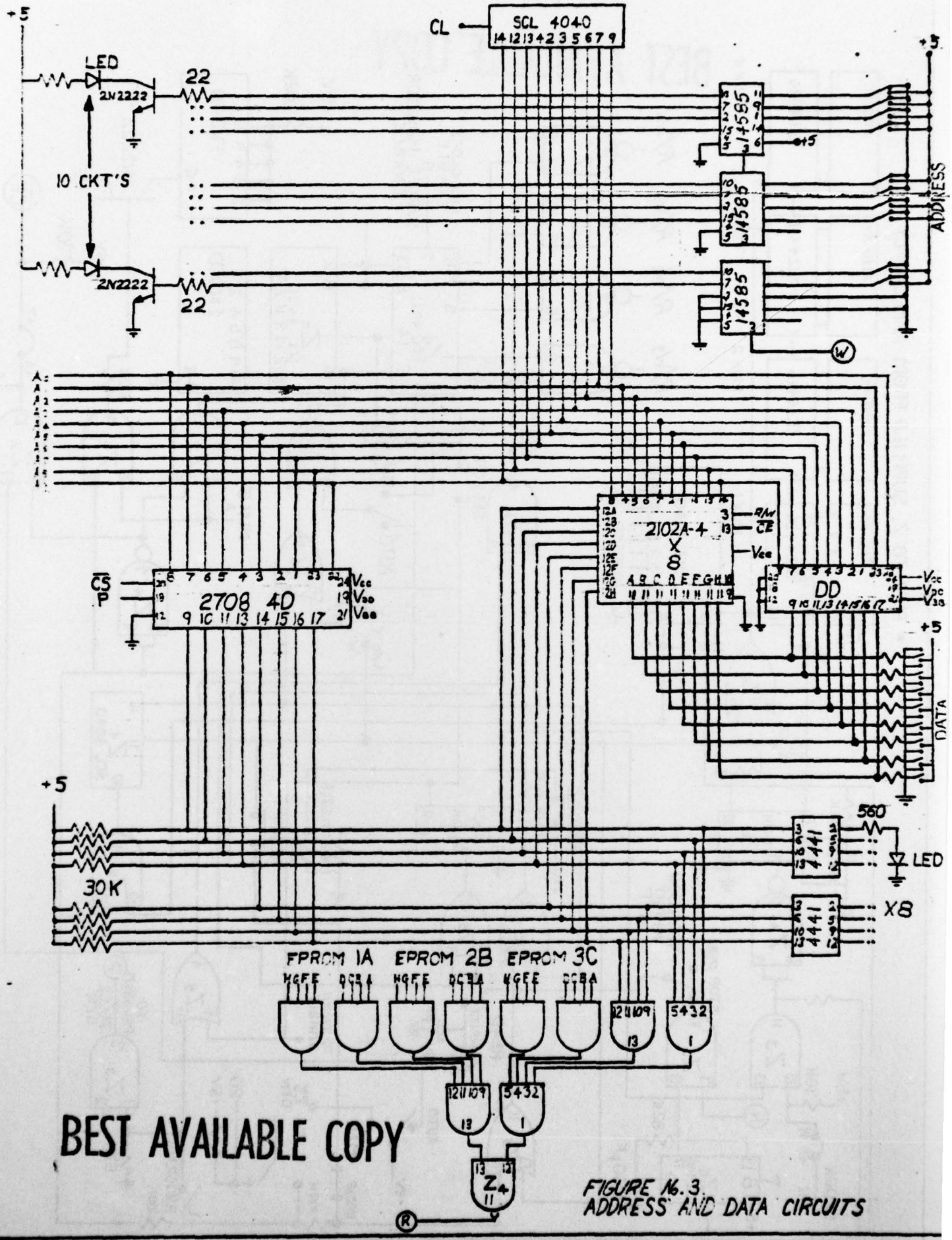


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FIGURE N6.3.
ADDRESS AND DATA CIRCUITS

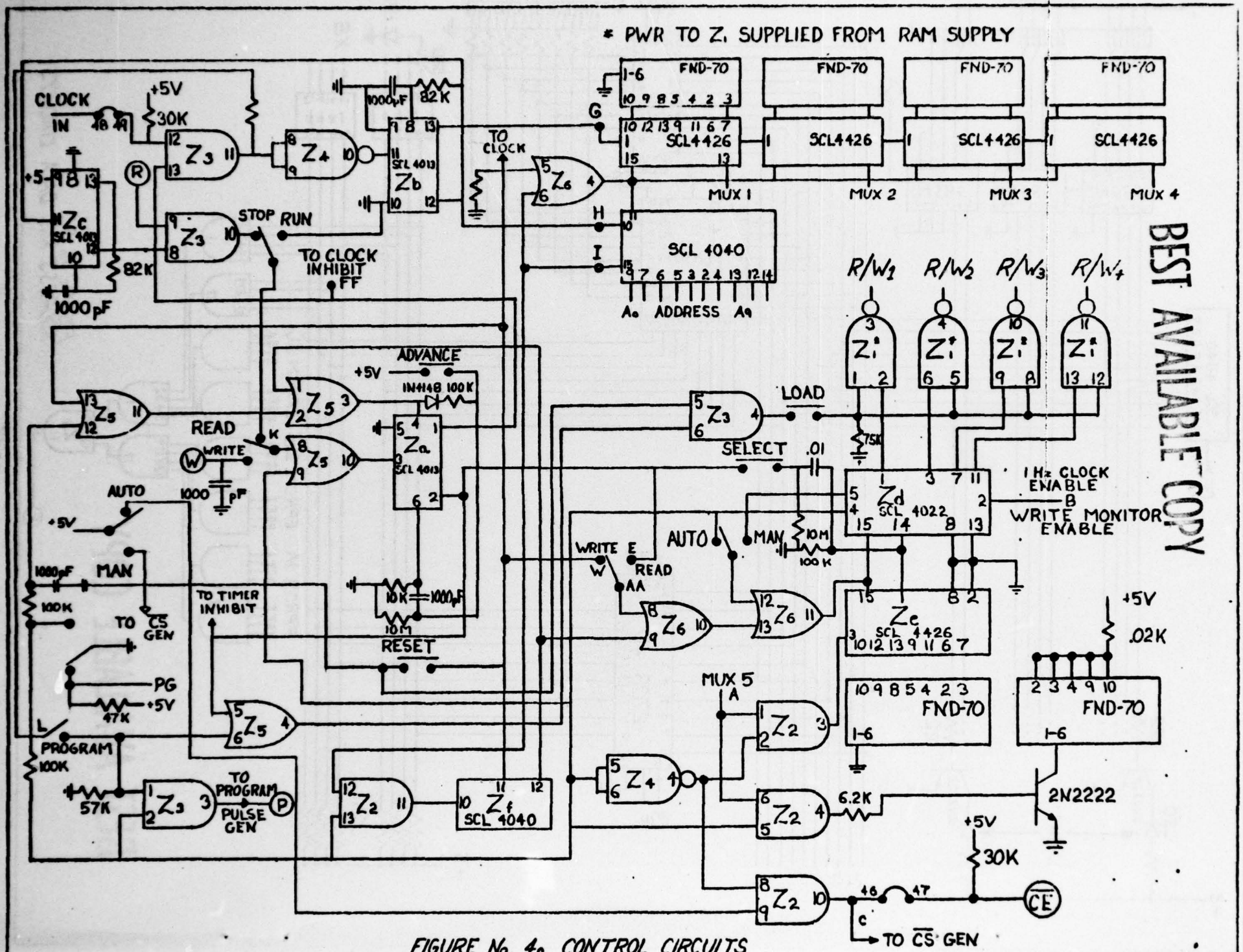


FIGURE No. 4a CONTROL CIRCUITS

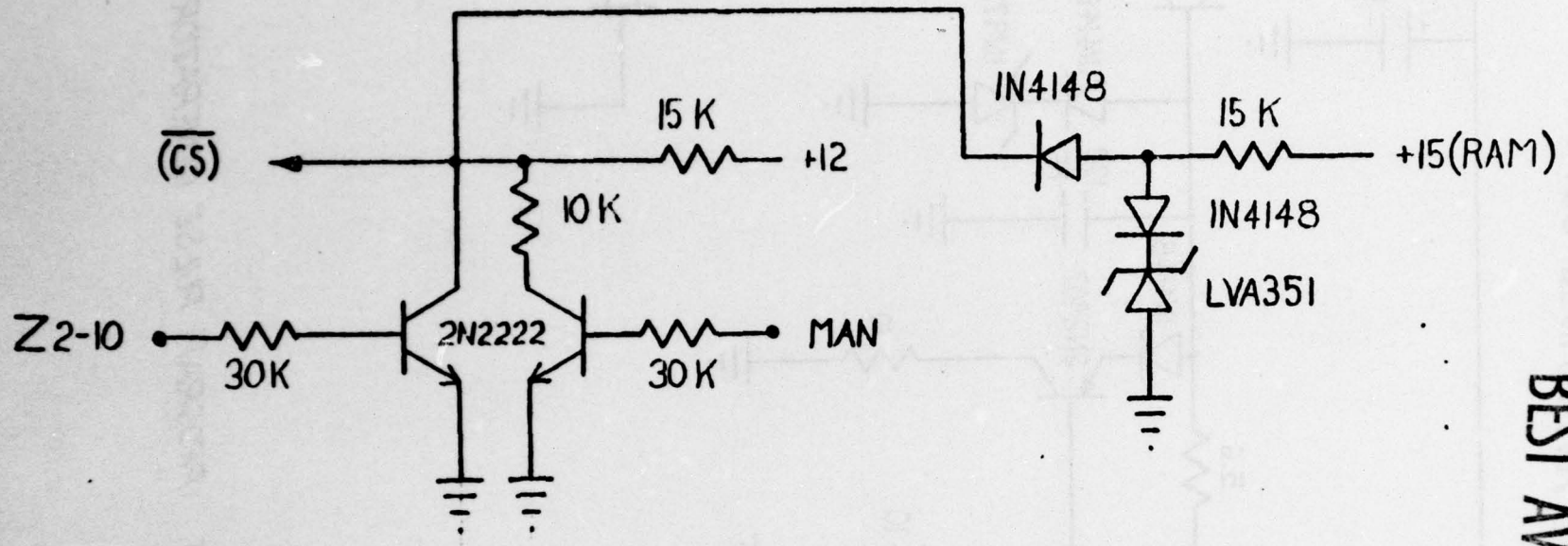


FIGURE No. 46 $\overline{CS}$ GENERATOR

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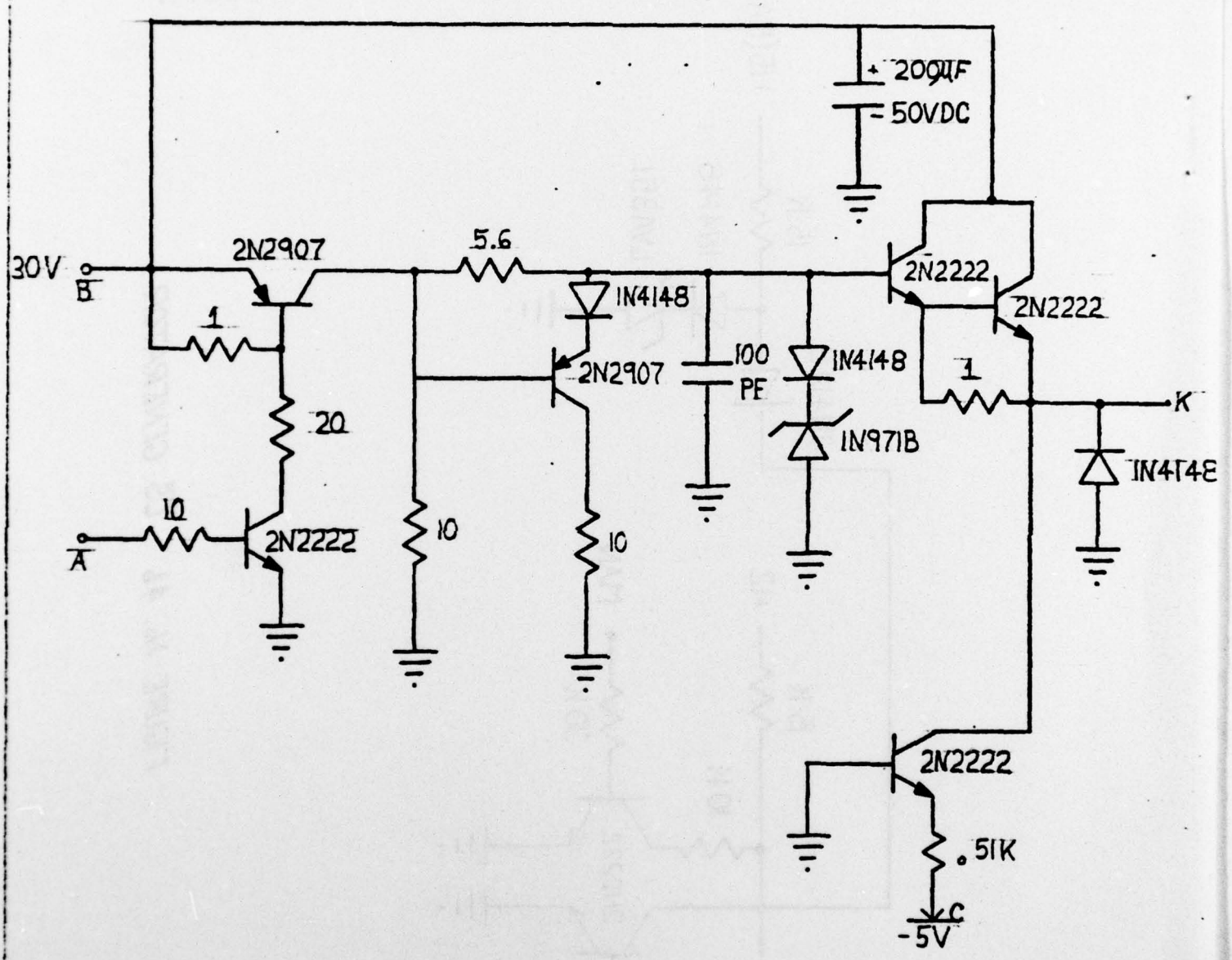


FIGURE No. 5. PROGRAM PULSE GENERATOR

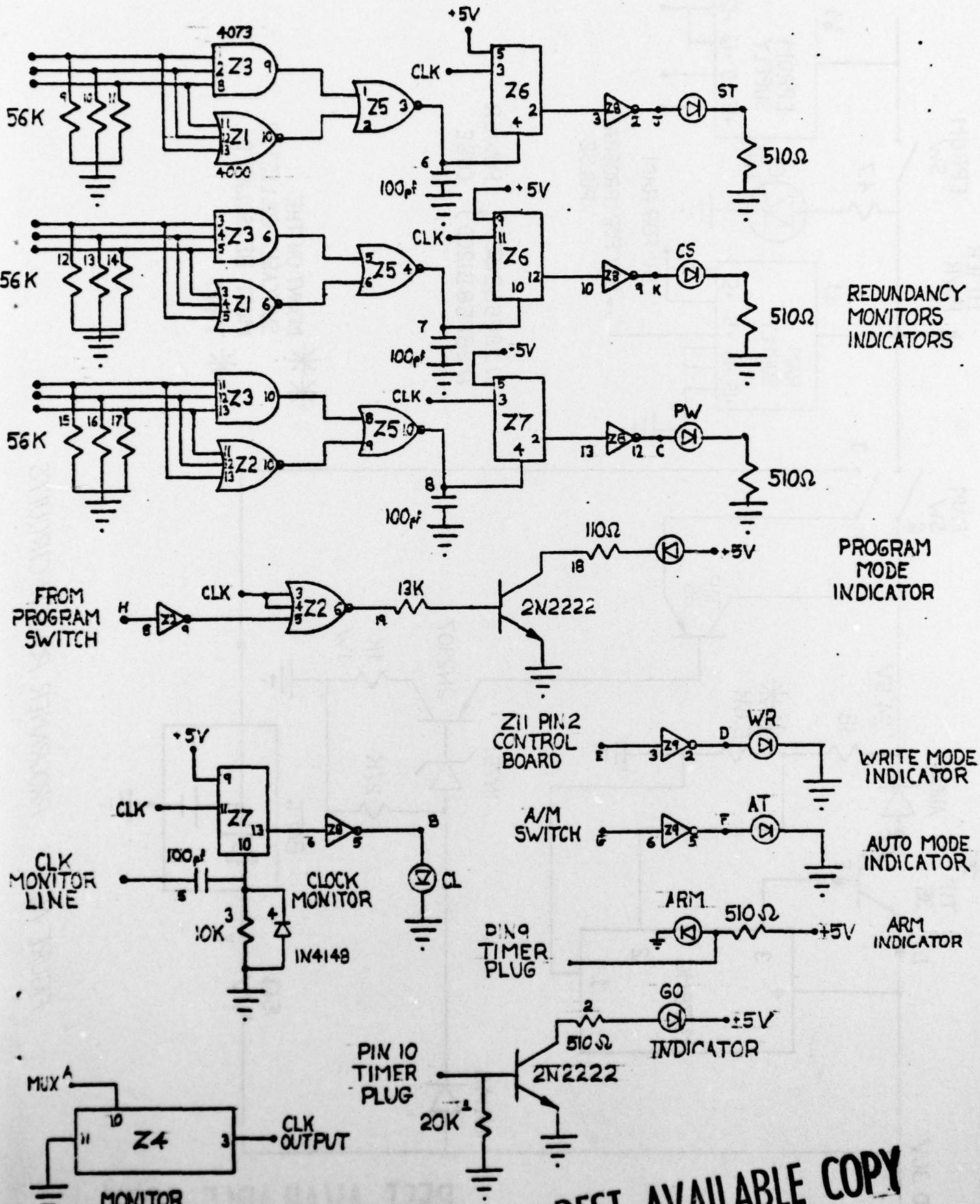


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FIGURE No. 6 MONITORS

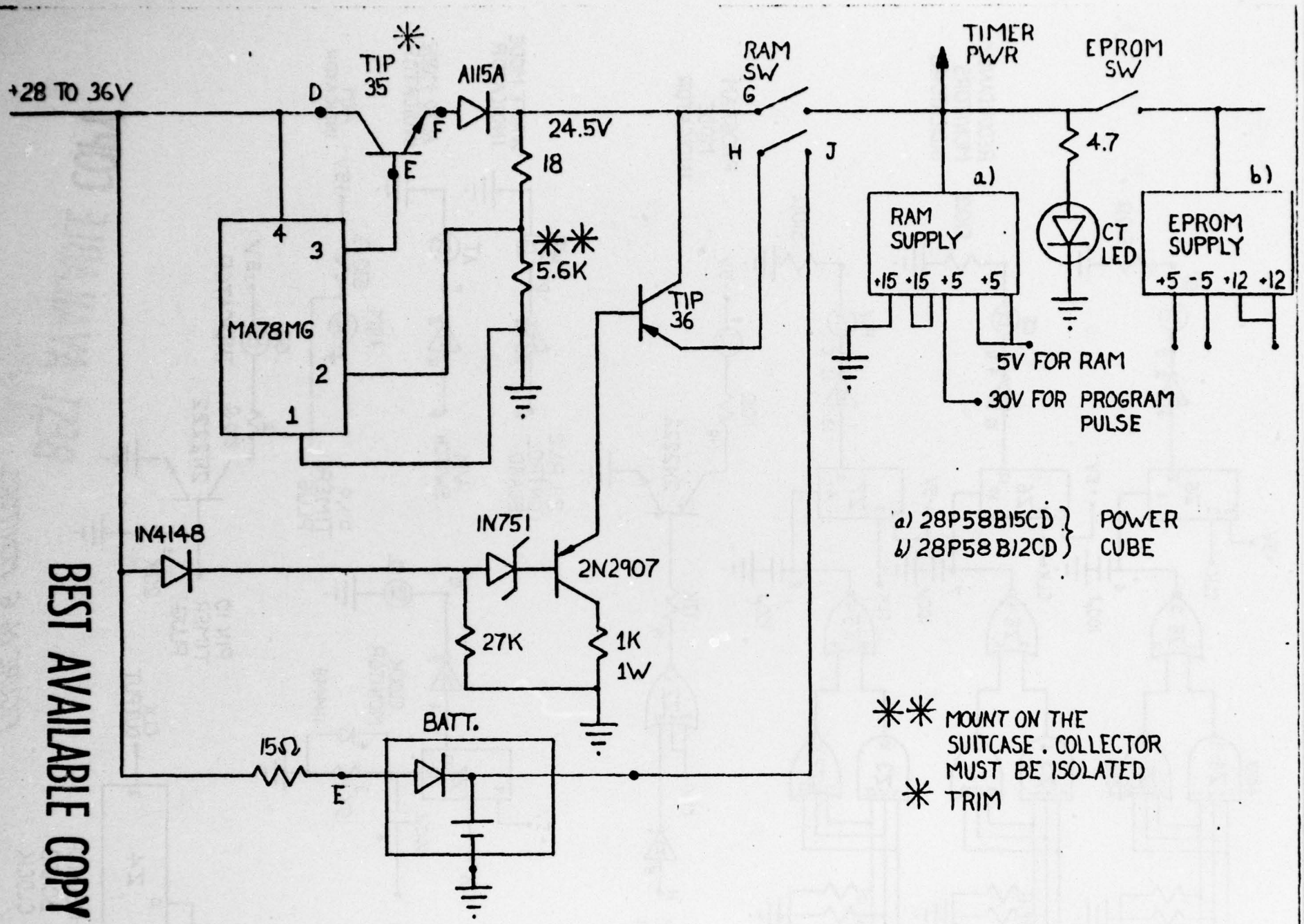


FIGURE No. 7 PROGRAMER POWER CIRCUITS

## PERSONNEL

A list of engineers and technicians who contributed to the work reported is given below:

Raimundas Sukys, Senior Research Associate, Engineer

Thomas Palasek, Research Fellow, Engineer

Christian Hazard, Technician, Electrical Engineering

Charles B. Sweeney, Technician, Electrical Engineering

## RELATED CONTRACTS

| | |
|---|---|
| F19628-67-C-0223 | 1 April 1967 through 28 February 1970 |
| F19628-70-C-0194 | 1 March 1970 through 28 February 1973 |
| F19628-73-C-0152 | 1 March 1973 through 30 April 1976 |
| F19628-76-C-0152 | 1 May 1976 through present |